SILICON PHOTOVOLTAICS R&D

Within its silicon photovoltaics R&D activities imec aims to explore and develop advanced process technologies to fuel the continuous market growth of silicon solar cells and modules in a sustainable way. The research concentrates on increasing cell and module energy conversion efficiency while optimizing manufacturing processes and material usage, thus significantly decreasing the cost per Watt. In order to achieve this, imec brings together silicon solar cell and module manufacturers, and equipment and material suppliers to create an industrial ecosystem.

WHAT WE OFFER

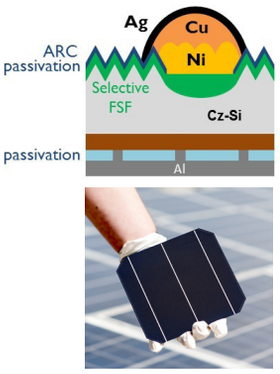
INDUSTRIAL SILICON SOLAR CELLS AND MODULE RESEARCH AND DEVELOPMENT

Imec builds innovative solar cell devices and module concepts, new processing technologies, equipment & material screening with partners, and other disruptive technology development, following our own roadmap and based on partners' request. The goal is to improve cell efficiency to more than 25% and to further lower manufacturing cost for next generation silicon solar cells. This research complements and enhances the partners' existing proprietary technologies. Imec's research is based on a track record of 30 years industrial PV research and innovation.

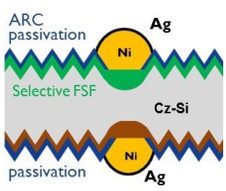
STATE-OF-THE-ART RESEARCH FACILITIES

Imec is currently undergoing a pre-pilot line for silicon solar cells (S-line, 1000m2). The goal is to develop and refine solar cell processes until they are ready to be further integrated into production lines. The equipment is similar to that of a state-of-the-art solar cell production environment and the batch size is large enough to allow valid predictions about averages, standard variations and yield. Techniques used in the cell pre-pilot line include isotropic acidic and KOH texturing, advanced wet chemical cleaning, single side wafer etching and polishing, POCl3 diffusion and oxidation furnaces, large area PECVD deposition of Si nitride, belt furnace rapid thermal anneal, in-line ALD, screenprinting, metal plating, a flexible laser platform, a-Si deposition and epitaxial growth of c-Si and poly-Si layers.

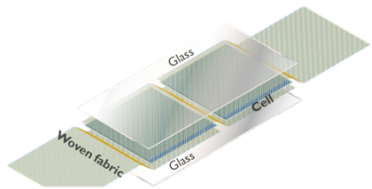
For PV modules, state of the art module assembly, testing and characterization techniques are available.



Mono-facial cell development



Bi-facial cell development



Novel module interconnect technology

MONO-FACIAL CELL DEVELOPMENT 22-24% EFFICIENCY

DEVELOPMENTS FOCUS ON THE REALIZATION OF HIGH EFFICIENCY CRYSTALLINE SI CELLS

- Design, modeling, processing and characterization, including reliability
- P-type or n-type platforms
- Step by step improvement implementation, focusing on: low cost efficient cleaning, passivation, 'TOPCON',metallisation,...
- Using standard wafers or kerfless wafers grown with epitaxy and build-in junctions.

SCREENPRINTED OR PLATED NPERT CELLS

- 22.9% best large area cell efficiency
- n-type or p-type Cz-Si wafers (156mm)
- Fine-line screenprinted or low-cost Ni/Cu co-plated metallization on both sides simultaneously
- Front Surface Field with dielectric passivation
- Rear side emitter (diffusion, epitaxy, heterojunction)
- Rear dielectric passivation (SiO2, Al2O3)
- Laser opened front and rear contacts

SCOPE

- Cost effective and up-scalable processing on standard p- or n-type wafers or kerfless wafers grown with epitaxy with build-in junctions
- Stability and reliability evaluation
- Towards 24% efficiency with simplified process

BI-FACIAL CELL DEVELOPMENT 22-25% EFFICIENCY

DEVELOPMENTS FOCUS ON THE DEVELOPMENT OF HIGH EFFICIENCY AND EXTREME BI-FACIALITY

- Design, modeling, processing and characterization
- Step by step improvement implementation
  focusing on: low cost efficient cleaning, passivation, 'TOPCON', metallisation, ...
- Using standard wafers or kerfless wafers grown with epitaxy and build-in junctions

NPERT CELLS WITH CLOSE TO 100% BI-FACIALITY

- 22.8% best large area cell efficiency (standard front-side test conditions on non-reflective chuck)
- 98% bifaciality, yielding a potential of effective efficiencies beyond 26%
- n-type or p-type Cz mono-Si (156 mm)
- Rear or front junction cell
- Fine-line screenprinted or low-cost Ni/Cu co-plated metallization on both sides simultaneously

SCOPE

- Cost effective and up-scalable processing on standard p- or n-type wafers or kerfless wafers grown with epitaxy with build-in junctions
- Stability and reliability evaluation
- Towards 25% efficiency with simplified process

NOVEL MODULE INTERCONNECTION TECHNOLOGY

DEVELOPMENTS COVERING

- Evaluation, characterization and reliability analysis of new module materials and cell types taking into account various weather conditions
- Module process optimization
- Integrated module technologies using low cost, low stress, low loss wire-based interconnections
- Novel woven interconnect module lamination and integration technology

SCOPE

- Module assembly
- Evaluation, analysis and characterization
- Innovative technology solution development
- Improved energy yield prediction models

partner in EnergyVille

CONTACT US

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